SFxxx-S PID Test Report (Potential Induced Degradation) TUV Rheinland Japan

ARC Product Management
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SOLAR FRONTIER

Outline

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What is PID?

PID (Potential Induced Degradation)

High Voltage Stress (HVS) is applied between frame and panel.

➔ The material becomes more conductive.

➔ Leakage current occurs within the solar panel

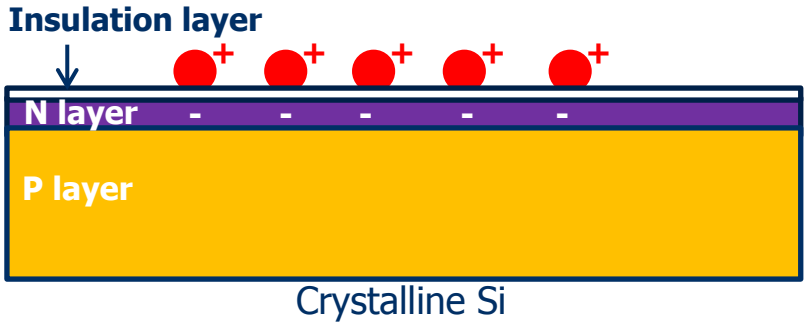
➔ Power degradation occurs

SF CIS modules PID free

Principle of PID & resistance of our CIS against PID

Principle of PID

High Voltage Stress (HVS) is applied between frame and panel.
➔ The positively charged sodium ions in the cover glass migrate to the insulation layer.
➔ At the same time, N layer is charged negatively due to the Na^+, and reverse bias occurs.
➔ Then, the excess charge triggers a "break down" where the shunt resistance and the open circuit voltage are dramatically reduced.



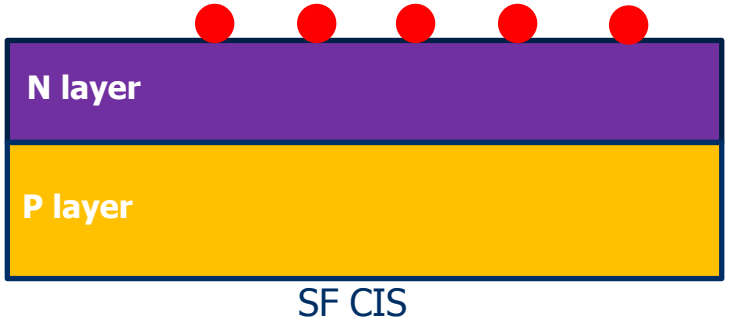
Crystalline Si

1) Insulation layer as anti-reflective layer (SiN etc.)
2) Thin N layer

Resistance of our CIS against PID

Why does our CIS have resistance against PID?

1) **There is no insulation layer, and therefore the reverse bias hardly occurs.**
2) **Even if the surface of N layer is charged, this doesn't trigger a break down because the N layer of our CIS is much thicker than that of crystalline Si.**

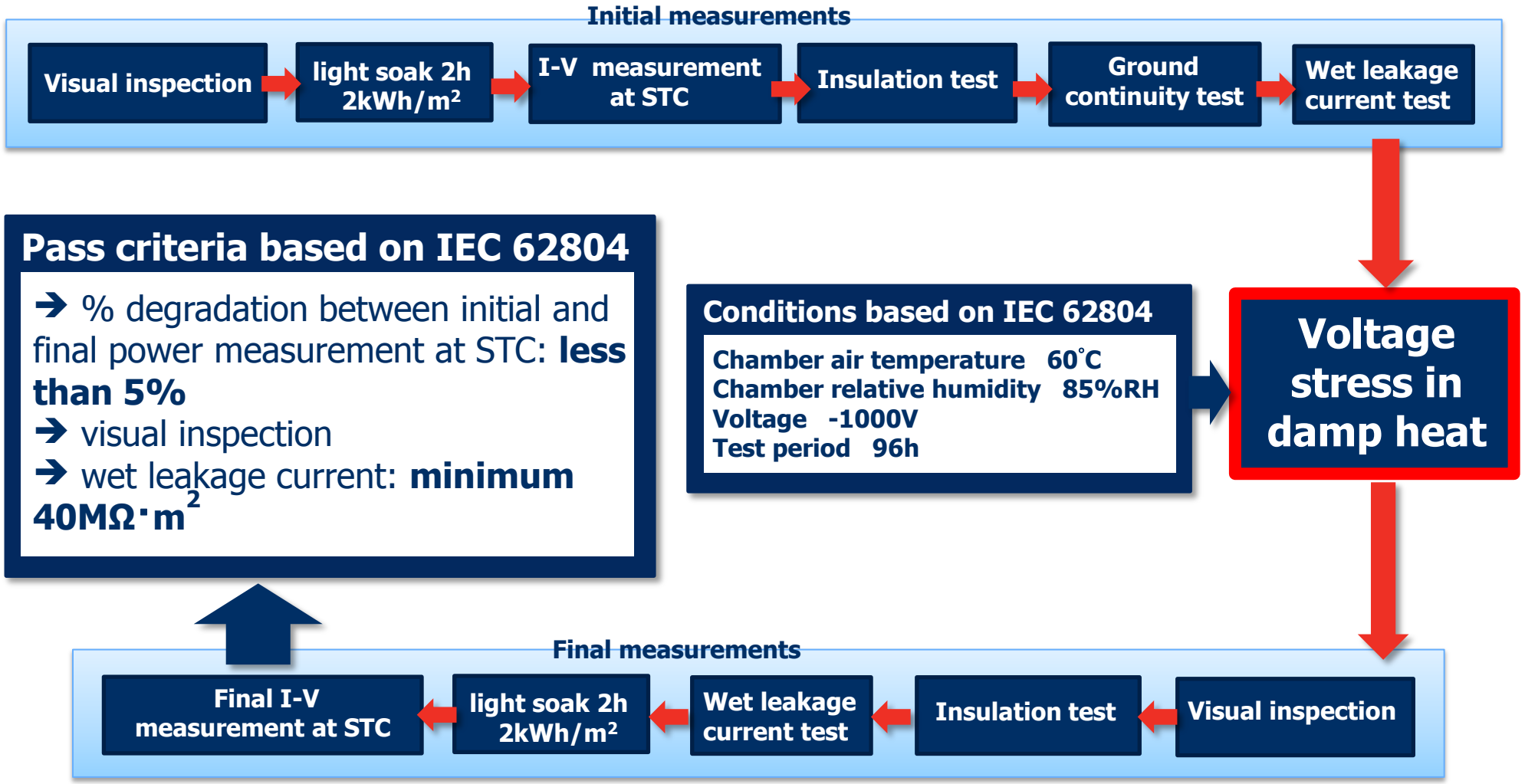


Our CIS

1) No insulation layer
2) Thick N layer

PID test @ TUV Japan based on IEC 62804 standard draft

Customized test sequence (two SF160 modules per condition)



Note: All steps refer to the document IEC 61646 except for voltage stress in damp heat (procedure outlined in IEC 62804 draft) and ground continuity test (IEC 61730-2).

TUV lab PID test result

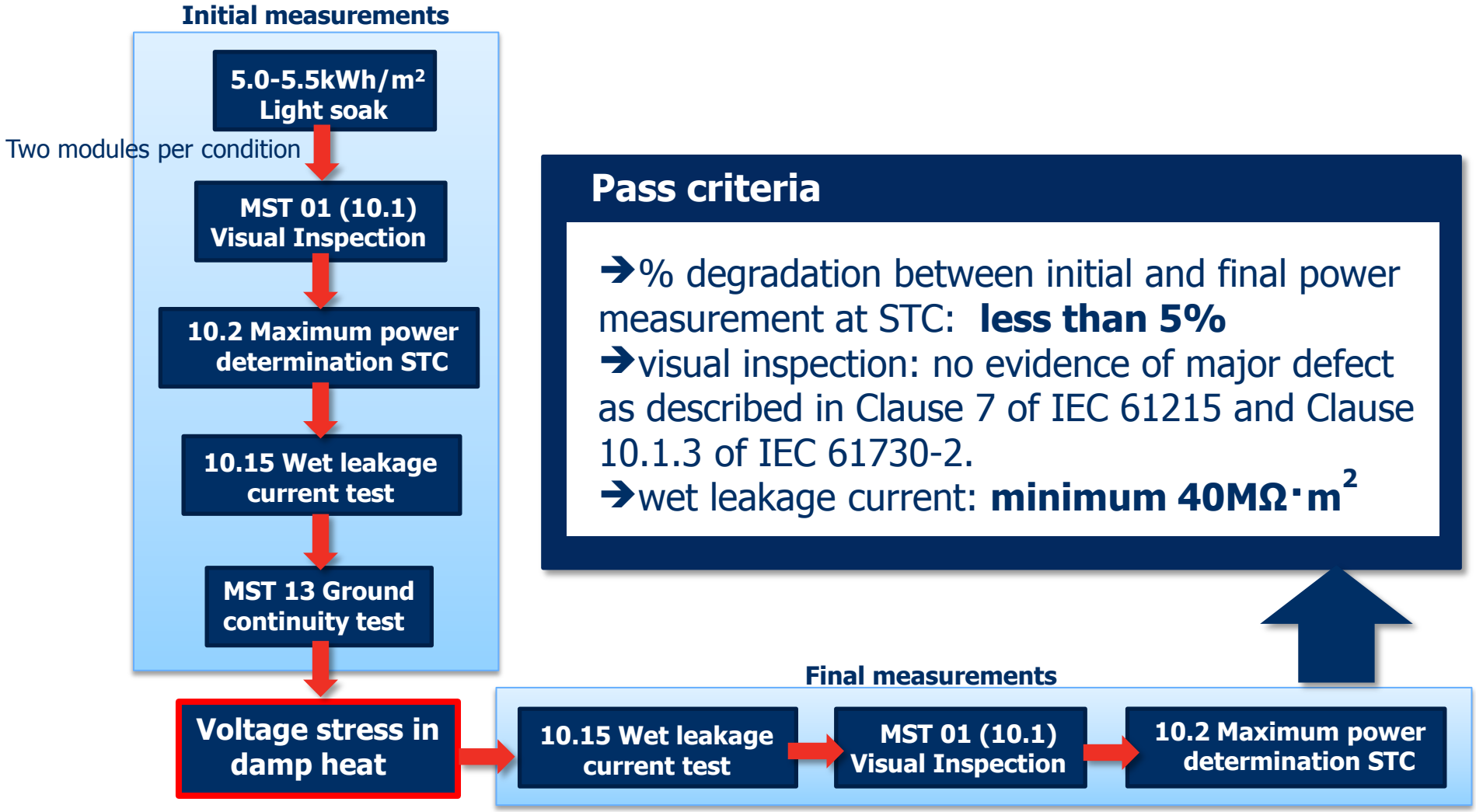
Sample #	Degradation (%)
A	- 0.06%
B	-0.72%

power measurement pass criteria : % degradation between initial and final power measurement
less than 5%

Zero % power degradation due to PID.
Power increase due to the unique light-soaking effect of SF CIS module is evident.

APPENDIX

IEC 62804 standard draft: *System voltage durability test for crystalline silicon modules-design qualification and type approval*

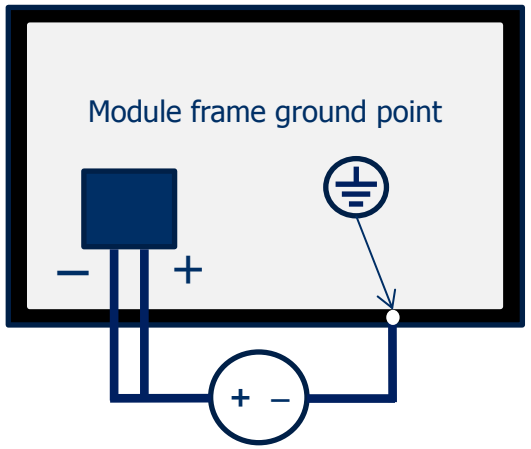


Notes: Steps 10.1, 10.2 and 10.15 refer to the document IEC 61215 ed.2
Steps MST 01 and MST 13 refer to the document IEC 61730-2

IEC 62804 standard draft: Test Condition

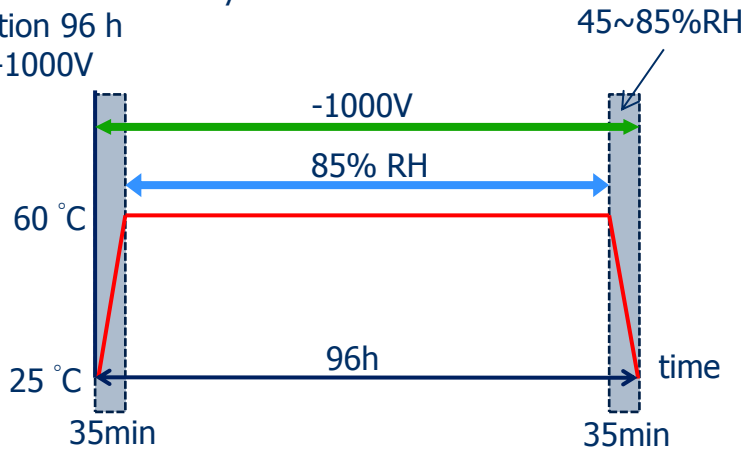
Test Condition: Voltage stress to modules in damp heat environment

a. The module shall be mounted into an environmental chamber with a non-porous electrically insulating mounting material.
b. Positive and negative connectors shall be connected to one another and to the high voltage terminal of the power supply.
c. The ground terminal of the high voltage power supply shall be connected with the module grounding point of the module.



d. Stresses are applied in chamber according to stress levels. The specified voltage will be applied during the ramp between the stress level from and to ambient condition. Relative humidity shall be maintained between 45% and 85% during the ramp.

Stress levels/severities
Chamber air temperature 60 ˚C ± 2 ˚ C
Chamber relative humidity 85 % ± 5 % RH
Test duration 96 h
Voltage: -1000V



e. Perform IEC 61215 ed 2 10.15 wet leakage current test between two and four hours after completion of step d.
f. Perform IEC 61215 ed 2 maximum power determination within 8 h after completion of step d and maintain the modules at ambient with maximum of 25° C.